Single Channel Synchronous Buck PWM Controller

Features

- **Single 12V Power Supply Required**
- **Excellent Output Voltage Regulation**
  - 1.0V ± 0.8% Internal Reference
- **Simple Single Loop Control Design-**
  Voltage Mode PWM Control
- **0~100% Duty Ratio**
- **Programmable Frequency Range from 80kHz to 300kHz**
- **Synchronous Switching Frequency Input**
- **Integrated Boot-Strap Diode**
- **Over-Current Protection**
  - Sense High-Side MOSFET's $R_{DS(ON)}$
- **Over-Voltage Protection**
- **Under-Voltage Protection**
- **Over-Temperature Protection**
- **Fault Indicator**
- **Available in SOP-14 Packages**
- **Halogen and Lead Free Available**
  (RoHS Compliant)

Applications

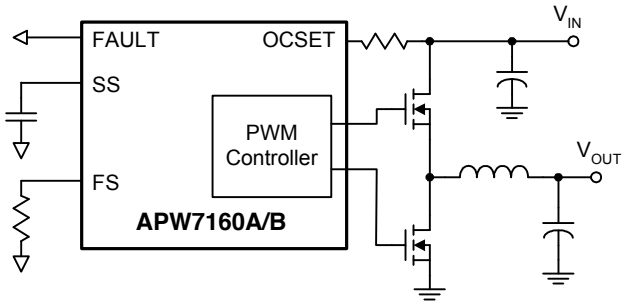
- **SMPS**

General Description

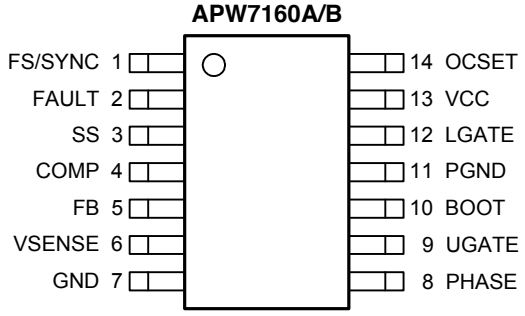
The APW7160A/B is a voltage mode and synchronous PWM controller which drives dual N-channel MOSFETs. The device integrates all of the control, monitoring, and protecting functions into a single package, provides controlled power output with over-voltage, under-voltage, over-temperature, and over-current protections.

The APW7160A/B provides excellent regulation for output load variation. The internal 1.0V temperature-compensated reference voltage provides high accuracy of 0.8%. The APW7160A/B has been equipped with excellent protection functions: POR, UVP, OCP, OTP, and OVP protections. The Power-On-Reset (POR) circuit can monitor the VCC and OCSET voltage to make sure the supply voltage exceeds their threshold voltage while the controller is running. The Over-Current Protection (OCP) monitors the output current by using the voltage drop across the high-side MOSFET's $R_{DS(ON)}$. When the output current reaches the trip point, the controller will be latched. Over-Voltage Protection (OVP) protects the IC from burnout when output voltage is 120% of normal output voltage. The oscillator frequency of APW7160A is single of FS input signal and APW7160B is double.The fault indicator monitors the device if any fault condition as above occurred. The APW7160A/B is available in SOP-14 packages.

Simplified Application Circuit



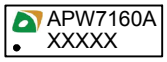
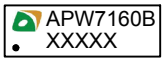
Pin Configuration



SOP-14 (Top View)

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APW7160A APW7160B □□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code K : SOP-14 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7160A K: 	XXXXX - Date Code
APW7160B K: 	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{VCC}	Input Bias Supply Voltage (VCC to GND)		-0.3 ~ 20	V
	BOOT to PHASE Voltage		-0.3 ~ 20	V
	UGATE to PHASE	<400ns pulse width	-5 ~ V_{BOOT}+5	V
		>400ns pulse width	-0.3 ~ V_{BOOT}+0.3	V
	LGATE to PGND Voltage	<400ns pulse width	-5 ~ V_{VCC}+0.3	V
		>400ns pulse width	-0.3 ~ V_{VCC}+0.3	V
	PHASE to PGND Voltage	<400ns pulse width	-10 ~ 32	V
		>400ns pulse width	-0.3 ~ 20	V
	OCSET, FS		-0.3 ~ 20	V
	SS, COMP, FAULT, FB, VSENSE to GND Voltage		-0.3 ~ 7	V
	PGND to GND Voltage		-0.3 ~ 0.3	V
P_D	Power Dissipation		Internally Limited	W
	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds		260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2) SOP-14	160	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{VCC}	Input Bias Supply Voltage (VCC to GND)	10.8 ~ 13.2	V
V_{IN}	Converter Input Voltage	7 ~ 13.2	V
I_{OUT}	Converter Output Current	0 ~ 30	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3 : Refer to the typical application circuit.

Electrical Characteristics

These specifications apply over V_{IN}=12V, V_{OUT}= 3.3V and T_A= 25 °C unless otherwise specified.

Symbol	Parameter	Test Conditions	APW7160A/B			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
	VCC Supply Current (Shutdown mode)		-	2	4	mA
I_{VCC}	VCC Supply Current	UGATE1/UGATE2 and LGATE1/LGATE2 open	-	5	12	mA
POWER-ON-RESET (POR) AND LOCKOUT VOLTAGE THRESHOLDS						
	Rising VCC Threshold		9	9.5	10	V
	Falling VCC Threshold		7.5	8	8.5	V
	Rising V_{OCSET} Threshold		-	5.5	-	V
	Falling V_{OCSET} Threshold		-	4.5	-	V
OSCILLATOR						
F_{OSC}	Free Running Frequency	FS = NC	-	80	-	kHz
	Programmable Frequency Range	Connect Resistor form FS to GND	80	-	300	kHz
	FS Input PWM Frequency	APW7160A APW7160B	80	- -	300 150	kHz kHz
	FS Input PWM High Threshold		6	-	14	V
	FS Input PWM Low Threshold		0	-	1	V
	Total Frequency Accuracy		-10	-	10	%
V_{OSC}	Ramp Amplitude (Note 4)		-	2.5	-	V
	Duty Cycle		0	-	100	%
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage		0.992	1.0	1. 008	V
	FB Input Current	V_{FB} = 1.0V	-	-	0.1	μA

Electrical Characteristics (Cont.)

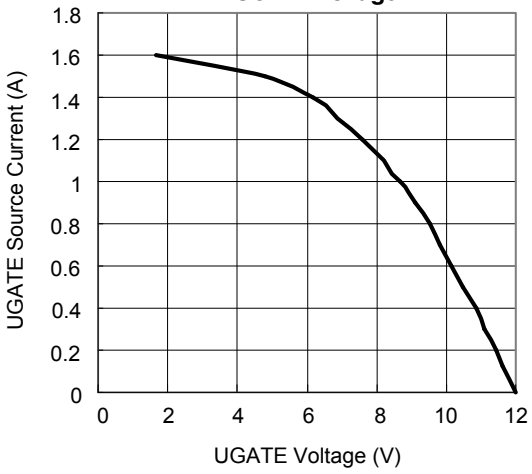
These specifications apply over V_{IN}=12V, V_{OUT}= 3.3V and T_A= 25°C unless otherwise specified.

Symbol	Parameter	Test Conditions	APW7160A/B			Unit
			Min.	Typ.	Max.	
PWM ERROR AMPLIFIERS						
	Open Loop Gain (Note 4)	R_L = 10kΩ, C_L = 10pF	-	88	-	dB
	Open Loop Bandwidth (Note 4)	R_L = 10kΩ, C_L = 10pF	-	15	-	MHz
	Slew Rate (Note 4)	R_L = 10kΩ, C_L = 10pF	-	6	-	V/μs
BOOT-STRAP DIODE AND SOFT-START						
V_F	Diode Forward Voltage	I_F = 10mA	-	1	-	V
I_R	Reversed Leakage Current	V_R=25V	-	0.2	0.5	μA
I_{SS}	Soft-Start Charge Current		24	30	36	μA
GATE DRIVES						
I_{UGATE}	Upper Gate Source Current	V_{BOOT} = 12V, V_{UGATE} – V_{PHASE} = 2V	-	1.6	-	A
I_{UGATE}	Upper Gate Sink Current	V_{BOOT} = 12V, V_{UGATE} – V_{PHASE} = 2V	-	1.2	-	A
I_{LGATE}	Lower Gate Source Current	V_{VCC} = 12V, V_{LGATE} = 2V	-	2	-	A
I_{LGATE}	Lower Gate Sink Current	V_{VCC} = 12V, V_{LGATE} = 2V	-	1.5	-	A
R_{UGATE}	Upper Gate Source Impedance	V_{BOOT} = 12V, I_{UGATE} = 0.1A	-	3.4	-	Ω
R_{UGATE}	Upper Gate Sink Impedance	V_{BOOT} = 12V, I_{UGATE} = 0.1A	-	1.5	-	Ω
R_{LGATE}	Lower Gate Source Impedance	V_{CC12} = 12V, I_{LGATE} = 0.1A	-	2.3	-	Ω
R_{LGATE}	Lower Gate Sink Impedance	V_{CC12} = 12V, I_{LGATE} = 0.1A	-	1.12	-	Ω
PROTECTION						
I_{OCSET}	OCSET Current Source		183	204	225	μA
	Over-Voltage on VSENSE		115	120	125	%V_{REF}
	Under-Voltage on VSENSE		45	50	55	%V_{REF}
	Over-Temperature Shutdown (Note 4)		-	150	-	°C
	Over-Temperature Hysteresis (Note 4)		-	40	-	°C
	FAULT Pin High Voltage	Source 5mA	4	-	-	V
	FAULT Pin Low Voltage	Sink 5mA	-	-	0.6	V

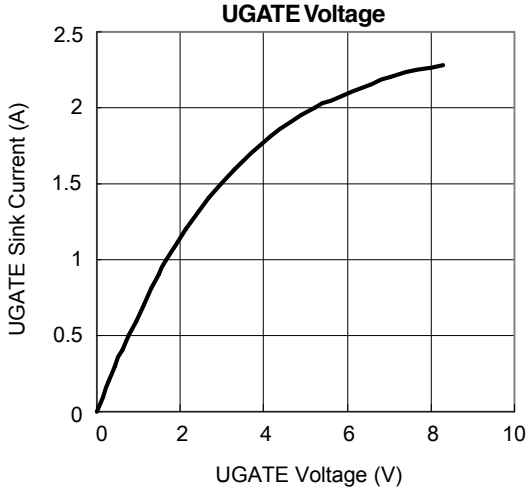
Note 4: Guarantee by design, not production test

Typical Operating Characteristics

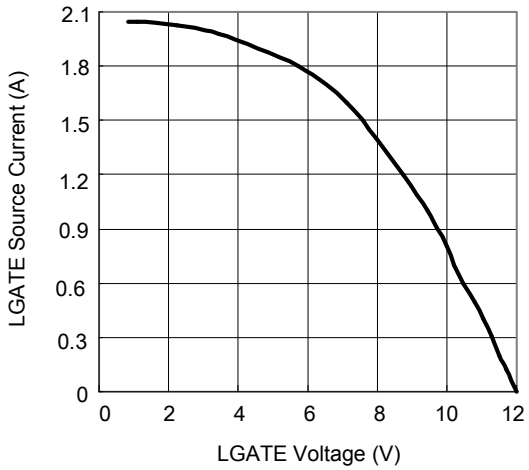
UGATE Source Current vs. UGATE Voltage



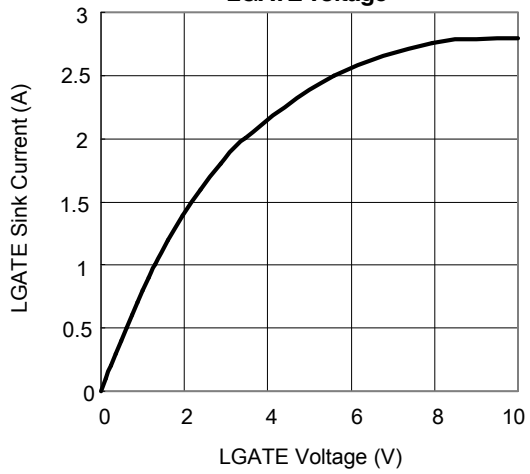
UGATE Sink Current vs. UGATE Voltage



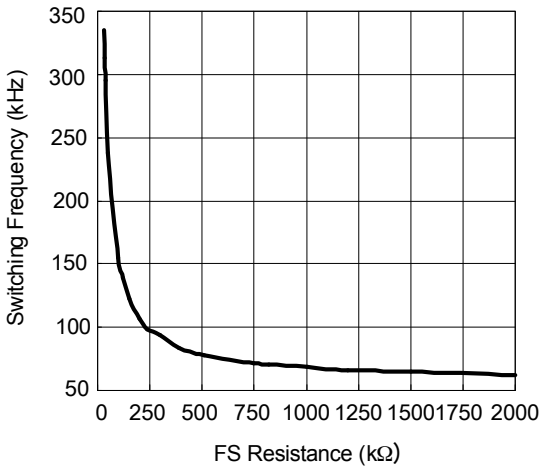
LGATE Source Current vs. LGATE Voltage



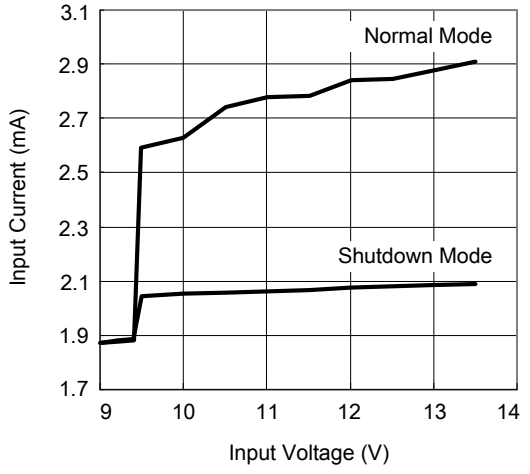
LGATE Sink Current vs. LGATE Voltage



Switching Frequency vs. FS Resistance



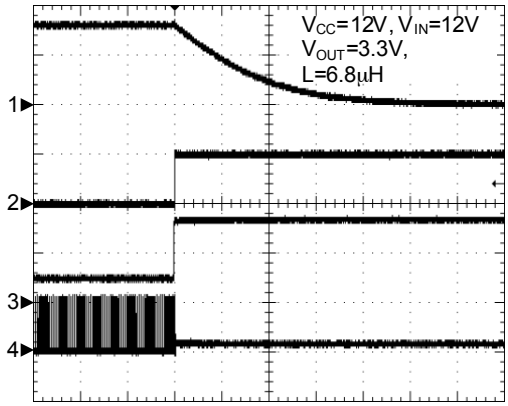
Input Voltage vs. Input Current



Operating Waveforms

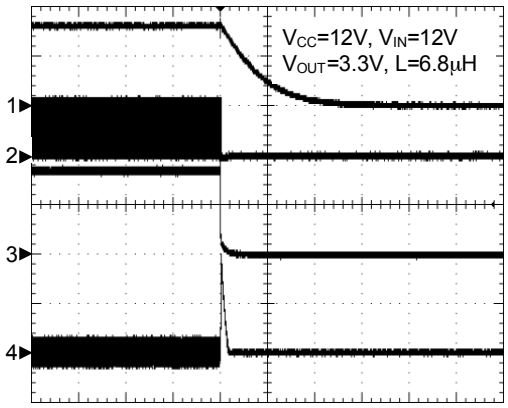
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

Over Voltage Protection



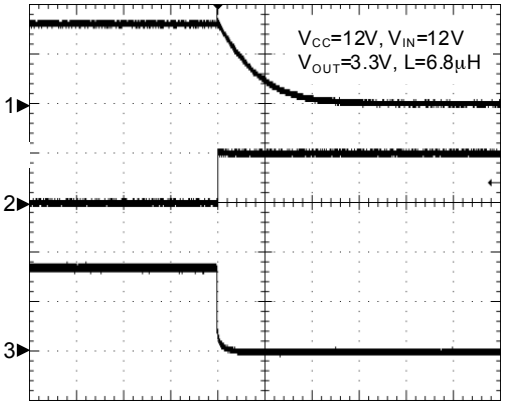
CH1: V_{SS} (2V/Div)
CH2: FAULT (5V/Div)
CH3: V_{SENSE} (2V/Div)
CH4: V_{UGATE} (20V/Div)
Time: 200μs/Div

Under Voltage Protection (1)



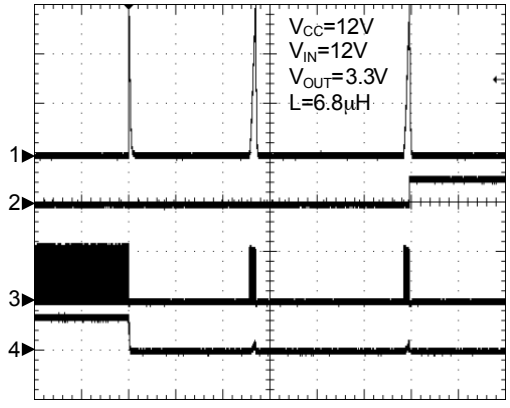
CH1: V_{SS} (2V/Div)
CH2: V_{UGATE} (20V/Div)
CH3: V_{OUT} (2V/Div)
CH4: I_L (5A/Div)
Time: 400μs/Div

Under Voltage Protection (2)



CH1: V_{SS} (2V/Div)
CH2: FAULT (5V/Div)
CH3: V_{OUT} (2V/Div)
Time: 400μs/Div

Over Current Protection

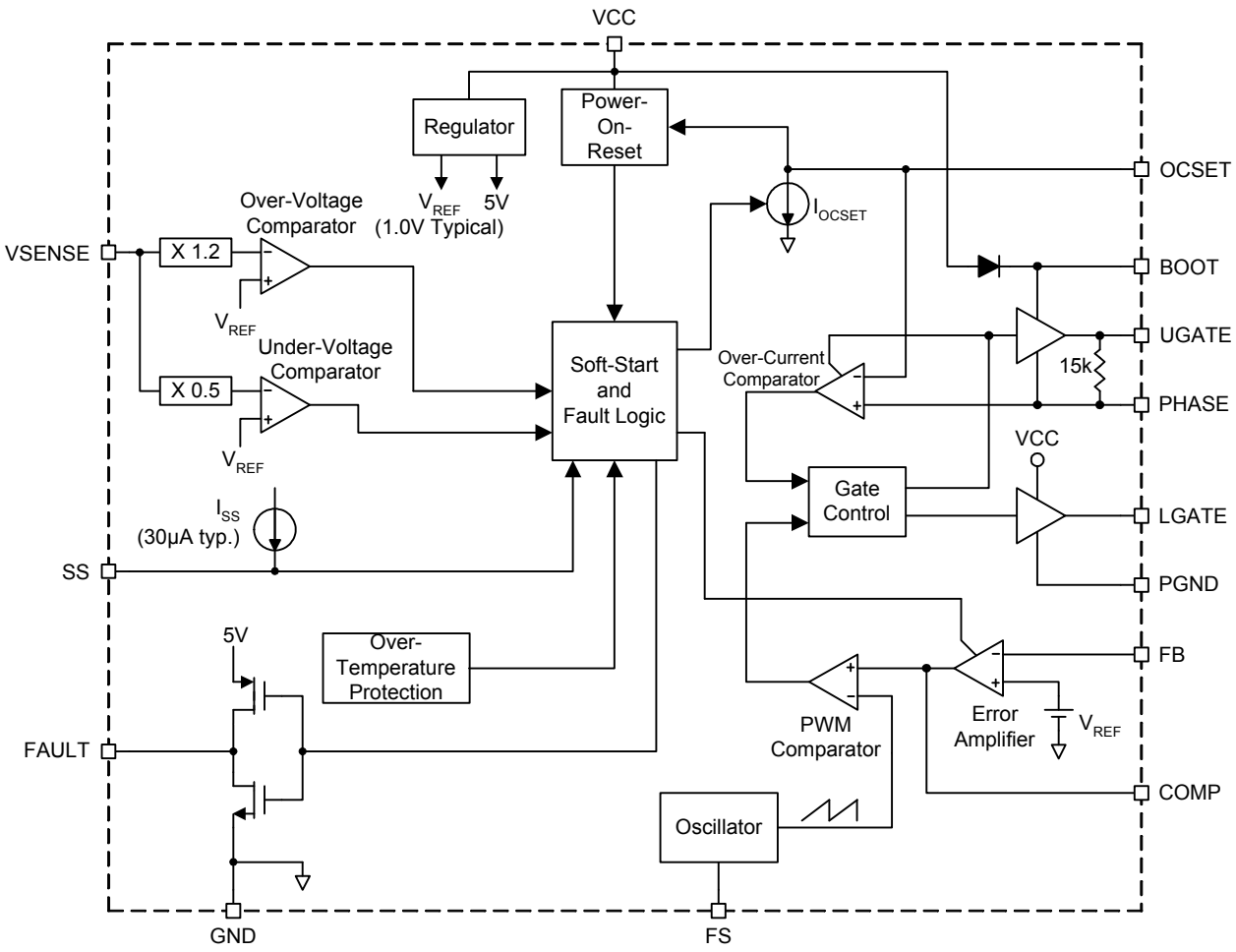


CH1: I_{OUT} (10A/Div)
CH2: FAULT (10V/Div)
CH3: V_{UGATE} (20V/Div)
CH4: V_{OUT} (5V/Div)
Time: 4ms/Div

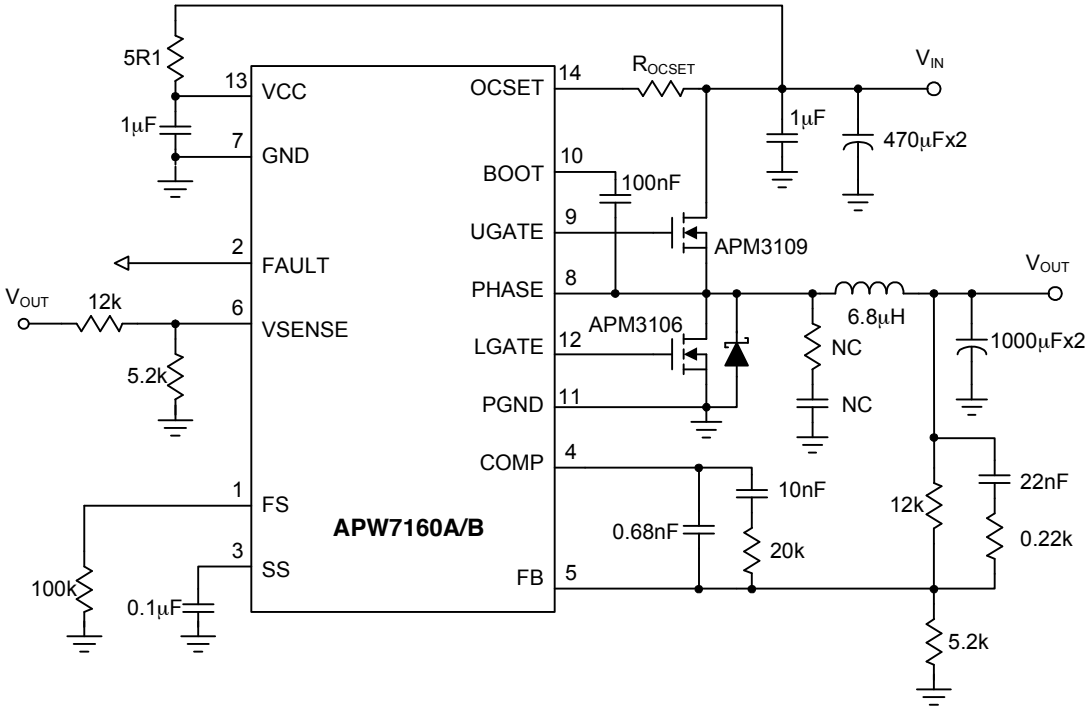
Pin Description

PIN		FUNCTION
NO.	NAME	
1	FS/SYNC	Frequency Setting and Synchronous Signal Input Pin. This pin is dual function input pin. Connect a resistor from FS to GND, setting the oscillating frequency of APW7160A/B. When a PWM signal input from this pin, the device is synchronously and operate with the input frequency. Refer to "Function Descriptions" for detail.
2	FAULT	Fault Indicator Output Pin. The APW7160A/B integrates extensive protection to fault conditions. Refer to "Function Description" for the detail. When any of these fault conditions was detected, this pin was pulled high to 5V (typical).
3	SS	Soft-Start Duration Input Pin. Connect a capacitor to the GND and a 30μA current source charges this capacitor to set the soft-start time. The pin also integrates EN/Shutdown function. Pulling SS below 0.7V shuts down the device.
4	COMP	Error Amplifier Output Pin. It is used to compensate the regulation control loop. Refer to the section "Application Information" for details.
5	FB	Feedback Input Pin. The Buck converter senses feedback voltage via FB and regulates the FB voltage at 1.0V. Connecting FB with a resistor-divider from the output sets the output voltage of the Buck converter.
6	VSENSE	Output Voltage Sense Pin. It is used to sense the output voltage. The VSENSE pin is the input of over-voltage and under-voltage comparator. When the voltage on VSENSE, V_{VSENSE}, exceed OVP threshold that is 120% of V_{REF}, the APW7160A/B turn off high-side and low-side MOSFETs. Connect a resistor diver from output to GND to set the OVP and UVP thresholds. VSENSE should not be left floating
7	GND	Signal Ground. Connecting this pin to PGND.
8	PHASE	This pin is the return path for the high-side gate driver. Connect this pin to the high-side MOSFET source and connect a capacitor to BOOT for the bootstrap voltage. This pin is also used to monitor the voltage drop across the MOSFET for over-current protection.
9	UGATE	Low-side Gate Driver Output. This pin is the gate driver for low-side MOSFET.
10	BOOT	This pin provides the bootstrap voltage to the high-side gate driver for driving the N-channel MOSFET. An external capacitor from PHASE to BOOT, an internal diode and the power supply voltage VCC generate the bootstrap voltage for the high-side gate driver (UGATE).
11	PGND	Power Ground of the Low-Side Gate Driver. Use a separate track to connect this pin to Source of the low-side MOSFET. The Source of the low-side MOSFET must be connected to system ground with very low impedance. Connecting this pin to GND.
12	LGATE	Low-side Gate Driver Output. This pin is the gate driver for low-side MOSFET.
13	VCC	Power Supply Input. Connect a nominal 10V to 13.2V power supply voltage to this pin. A power-on-reset function monitors the input voltage at this pin. It is recommended that a decoupling capacitor (1 to 10μF) should be connected to the GND for noise decoupling.
14	OCSET	This pin is used to set the maximum inductor current. Refer to the section in "Function Description" for detail.

Block Diagram



Typical Application Circuit



Function Description

VCC Power-On-Reset (POR)

The Power-On-Reset (POR) function of APW7160A/B continually monitors the voltage on VCC and OCSET pin. When the voltage on VCC and OCSET exceed their rising POR threshold voltage respectively (9.5V and 1.6V typical), the POR function initiates soft-start operation. Where the voltage at OCSET pin is equal to V_{IN} minus a fixed voltage drop ($V_{OCSET} = V_{IN} - V_{ROCSET}$). For operation with a single +12V power source, V_{IN} and VCC are equivalent and the +12V power source must exceed the rising VCC threshold. With all input supplies above their POR thresholds, the device initiates a soft-start interval.

If the V_{SS} below 0.7V, the APW7160A/B places the controller into shutdown mode which UGATE and LGATE are pulled to PHASE and GND respectively. When the pull-down device is released, the V_{SS} will start to rise. When the V_{SS} rises above 0.8V, the APW7160A/B will begin a new initialization and soft-start process.

$$T_{SOFT-START} = \frac{C_{SS}}{I_{SS}} \times 1V$$

Where C_{SS} = external capacitor connected at SS pin.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7160A/B. When the junction temperature exceeds 150°C, a thermal sensor pulls UGTAE and LGATE low, allowing the devices to cool. The thermal sensor allows the converters to start a soft-start process and regulate the output voltage again after the junction temperature cools by 40°C. The OTP is designed with a 40°C hysteresis to lower the average Junction Temperature (T_J) during continuous thermal overload conditions, increasing the lifetime of the device.

Current-Limit Protection (OCP)

The over-current circuit (OCP) protects the switching converter against over-current or short-circuit conditions. The controller senses the inductor current by detecting the drain-to-source voltage which is the product of the inductor's current and the on-resistance of the high-side MOSFET during it's on-state. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor required.

A resistor (R_{OCSET}) connected between OCSET pin and the drain of the high-side MOSFET will determine the over-current limit. An internal current source will flow through this resistor, creating a voltage drop, which will be compared with the voltage across the high-side MOSFET. When the voltage across the high-side MOSFET exceeds the voltage drop across the R_{OCSET} for 3 cycles passing time continuously even full duty, the IC shuts off the entire gate drives.

The device was shut down. The output of the PWM converter is latched to be floating**.** The threshold of the over-current limit is therefore given by:

$$I_{LIMIT} = \frac{I_{OCSET} \cdot R_{OCSET}}{R_{DS(ON)}(High-Side)}$$

For the over-current is never occurred in the normal operating load range, the variation of all parameters in the above equation should be determined.

- The MOSFET's $R_{DS(ON)}$ is varied by temperature and gate to source voltage, the user should determine the maximum $R_{DS(ON)}$ in manufacturer's datasheet.
- The minimum I_{OCSET} (183μA) and minimum R_{OCSET} should be used in the above equation.
- Note that the I_{LIMIT} is the current flow through the high-side MOSFET; I_{LIMIT} must be greater than maximum output current add the half of inductor ripple current.

An over-current event will shut down the device and discharge the C_{SS} with a 30μA sink current and then shutdown the device. The APW7160A/B will initiate a soft-start process until re-cycle power supply (10V typical). When the R_{OCSET} is not connected or the V_{OCSET} below 1.6V, the APW7160A/B will not initiate soft-start process.

Output Over-Voltage Protection (OVP)

The over-voltage protection (OVP) circuit monitors the VSENSE (V_{VSENSE}) voltage to prevent the output from over-voltage. When the V_{SENSE} rises to 120% of the reference voltage (V_{REF}), the APW7160A/B turns off, both high-side and low-side MOSFETs and shut off. The APW7160A/B will initiate a soft-start process until re-cycle power supply.

Output Under-Voltage Protection (UVP)

The under-voltage protection circuit monitors the voltage on VSENSE (V_{VSENSE}) by Under-Voltage (UV) comparator to protect the PWM converter against short-circuit

Function Description (Cont.)

Output Under-Voltage Protection (UVP) (Cont.)

conditions. When the V_{VSENSE} falls below the falling UVP threshold (50% V_{REF}), a fault signal is generated and the device turns off high-side and low-side MOSFETs. The converter shuts down and the output is latched to be floating.

Fault Indicator

The APW7160A/B integrates extensive protection to cover failure conditions. The failure conditions include output over-current, output over-voltage, and over-temperature. When any of above condition detected, the FAULT pin is pulled high to 5V (typical) and the APW7160 shuts down. Under normal operating, the internal push-pull circuit draw the FAULT voltage lower than 0.6V. The FAULT pin can be used as a coarse reference with few mA sourcing/ sinking capabilities.

Frequency Setting and Synchronous Input

The APW7160A/B allow two ways to set the oscillated frequency from FS pin. They are:
1. Connect a resistor from FS to GND.
2. A PWM signal input.

The APW7160A/B provides the oscillator switching frequency adjustment. Connect a resistor from FS pin to the ground to adjust the switching frequency.
Another way is the PWM signal input. When the signal input from FS, the APW7160A/B operates synchronously with the input frequency. The APW7160A/B turns high-side MOSFETs on when the PWM signal rising edge triggered. The operating frequency of APW7160A is single of FS input signal and APW7160B is double.

Application Information

Output Voltage Selection

The output voltage can be programmed with a resistive divider. Use 1% or better resistors for the resistive divider is recommended. The FB pin is the inverter input of the error amplifier, and the reference voltage is 1V. The output voltage is determined by:

$$V_{OUT} = 1 \times \left(1 + \frac{R_{OUT}}{R_{GND}}\right)$$

Where R_{OUT} is the resistor connected from V_{OUT} to FB and R_{GND} is the resistor connected from FB to the GND.

Output Inductor Selection

The inductor value determines the inductor ripple current and affects the load transient response. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

$$\Delta V_{OUT} = I_{RIPPLE} \times ESR$$

where Fs is the switching frequency of the regulator.

Although increase of the inductor value and frequency reduces the ripple current and voltage, a tradeoff will exist between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_S) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFET and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, select an inductor is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

Output Capacitor Selection

Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is intended for switching regulator applications. In some applications, multiple capacitors have to be parallel to achieve the desired ESR value. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors also must be considered. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer. For high frequency decoupling, a ceramic capacitor 1μF can be connected between the drain of upper MOSFET and the source of lower MOSFET.

MOSFET Selection

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reverse transfer capacitance (C_{RSS}) and maximum output current requirement. There are two components of loss in the MOSFETs: conduction loss and transition loss. For the upper and lower MOSFET, the losses are approximately given by the following equations:

$$P_{UPPER} = I_{OUT}^2 (1 + TC)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_S$$

$$P_{LOWER} = I_{OUT}^2 (1 + TC)(R_{DS(ON)})(1-D)$$

Where I_{OUT} is the load current

TC is the temperature dependency of $R_{DS(ON)}$

F_S is the switching frequency

t_{SW} is the switching interval

D is the duty cycle

Application Information (Cont.)

MOSFET Selection (Cont.)

Note that both MOSFETs have conduction loss while the upper MOSFET includes an additional transition loss. The switching internal, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The (1+TC) term is to factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs Temperature" curve of the power MOSFET.

PWM Compensation

The output LC filter of a step down converter introduces a double pole, which contributes with -40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network among COMP, FB, and V_{OUT} should be added. The compensation network is shown in Figure 4. The output LC filter consists of the output inductor and output capacitors. The transfer function of the LC filter is given by:

$$F_{ESR} = \frac{1}{2\times\pi\times ESR\times C_{OUT}}$$

The F_{LC} is the double poles of the LC filter, and F_{ESR} is the zero introduced by the ESR of the output capacitor.

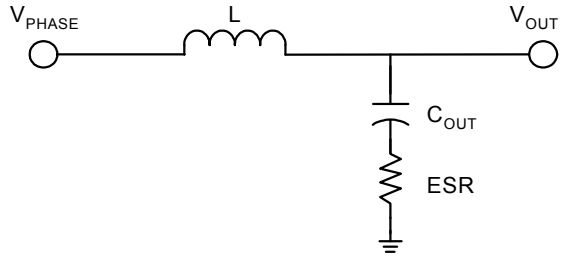


Figure 1. The Output LC Filter

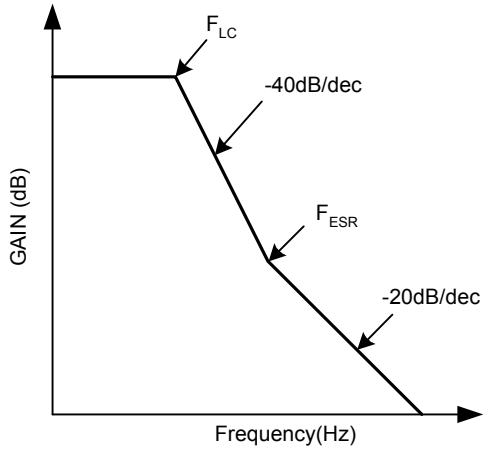


Figure 2. The LC Filter GAIN and Frequency

The PWM modulator is shown in Figure 3. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by:

$$GAIN_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

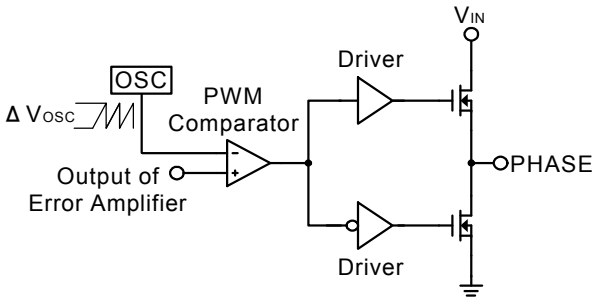


Figure 3. The PWM Modulator

The compensation network is shown in Figure 4. It provides a close loop transfer function with the highest zero crossover frequency and sufficient phase margin. The transfer function of error amplifier is given by:

$$GAIN_{AMP} = \frac{V_{COMP}}{V_{OUT}} = \frac{\frac{1}{sC1}//\left(R2+\frac{1}{sC2}\right)}{R1//\left(R3+\frac{1}{sC3}\right)}$$

$$= \frac{R1+R3}{R1\times R3\times C1}\times\frac{\left(s+\frac{1}{R2\times C2}\right)\times\left(s+\frac{1}{(R1+R3)\times C3}\right)}{s\left(s+\frac{C1+C2}{R2\times C1\times C2}\right)\times\left(s+\frac{1}{R3\times C3}\right)}$$

The poles and zeros of the transfer function are:

$$F_{Z1} = \frac{1}{2\times\pi\times R2\times C2}$$

$$F_{Z2} = \frac{1}{2\times\pi\times(R1+R3)\times C3}$$

$$F_{P1} = \frac{1}{2\times\pi\times R2\times\left(\frac{C1\times C2}{C1+C2}\right)}$$

$$F_{P2} = \frac{1}{2\times\pi\times R3\times C3}$$

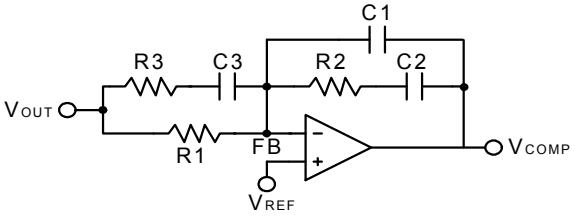


Figure 4. Compensation Network

Application Information (Cont.)

PWM Compensation (Cont.)

The closed loop gain of the converter can be written as:

$$GAIN_{LC} X\, GAIN_{PWM} X\, GAIN_{AMP}$$

Figure 5. shows the asymptotic plot of the closed loop converter gain, and the following guidelines will help to design the compensation network. Using the below guidelines should give a compensation similar to the curve plotted. A stable closed loop has a -20dB/ decade slope and a phase margin greater than 45 degree.

1. Choose a value for R1, usually between 1K and 5K.

2. Select the desired zero crossover frequency

$$F_O: (1/5 \sim 1/10)\ X\ F_S > F_O > F_{ESR}$$

Use the following equation to calculate R2:

$$R2 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{F_O}{F_{LC}} \times R1$$

3. Place the first zero F_{Z1} before the output LC filter double pole frequency F_{LC}.

$$F_{Z1} = 0.75\ X\ F_{LC}$$

Calculate the C2 by the equation:

$$C2 = \frac{1}{2 \times \pi \times R2 \times F_{LC} \times 0.75}$$

4. Set the pole at the ESR zero frequency F_{ESR}:

$$F_{P1} = F_{ESR}$$

Calculate the C1 by the equation:

$$C1 = \frac{C2}{2 \times \pi \times R2 \times C2 \times F_{ESR} - 1}$$

5. Set the second pole F_{P2} at the half of the switching frequency and also set the second zero F_{Z2} at the output LC filter double pole F_{LC}. The compensation gain should not exceed the error amplifier open loop gain, check the compensation gain at F_{P2} with the capabilities of the error amplifier.

$$F_{P2} = 0.5\ X\ F_S$$

$$F_{Z2} = F_{LC}$$

Combine the two equations will get the following component calculations:

$$GAIN_{LC} = \frac{1 + s \times ESR \times C_{OUT}}{s^2 \times L \times C_{OUT} + s \times ESR \times C_{OUT} + 1}$$

The poles and zero of this transfer functions are:

$$F_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}}$$

$$R3 = \frac{R1}{\frac{F_S}{2 \times F_{LC}} - 1}$$

$$C3 = \frac{1}{\pi \times R3 \times F_S}$$

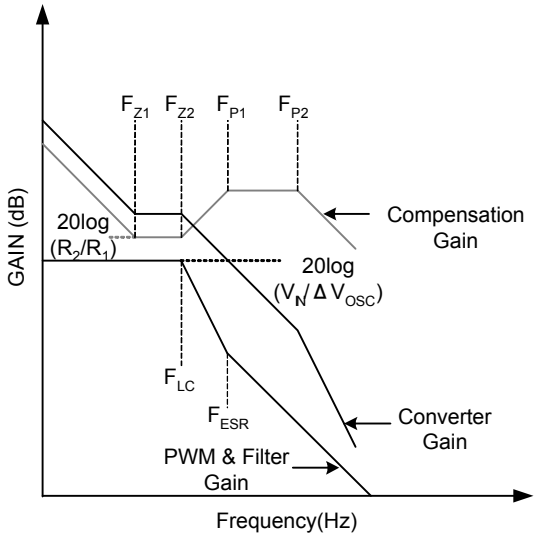


Figure 5. Converter Gain and Frequency

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at 200kHz, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is free-wheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. And signal and power grounds are to be kept separating till combined using the ground plane construction or single point grounding. Figure 6. illustrates the layout, with bold lines

Application Information (Cont.)

Layout Consideration (Cont.)

indicating high current paths; these traces must be short and wide. Components along the bold lines should be placed close together. Below is a checklist for your layout:

- Keep the switching nodes (UGATE, LGATE, and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible.
- The traces from the gate drivers to the MOSFETs (UGATE and LGATE) should be short and wide.
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node.
- Decoupling capacitor, compensation component, the resistor dividers, and boot capacitors should be close their pins. (For example, place the decoupling ceramic capacitor near the drain of the high-side MOSFET as close as possible. The bulk capacitors are also placed near the drain).
- The input capacitor should be near the drain of the upper MOSFET; the output capacitor should be near the loads. The input capacitor GND should be close to the lower MOSFET GND.
- The drain of the MOSFETs (VIN and PHASE nodes) should be a large plane for heat sinking.
- The R_{OCSET} resistance should be placed near the IC as close as possible.
- The decoupling capacitor for VCC should be placed near the VCC and GND. C_{BOOT} should be connected as close to the BOOT and PHASE pins as possible.

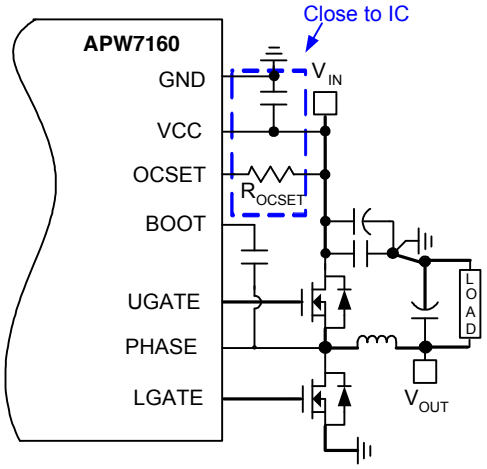
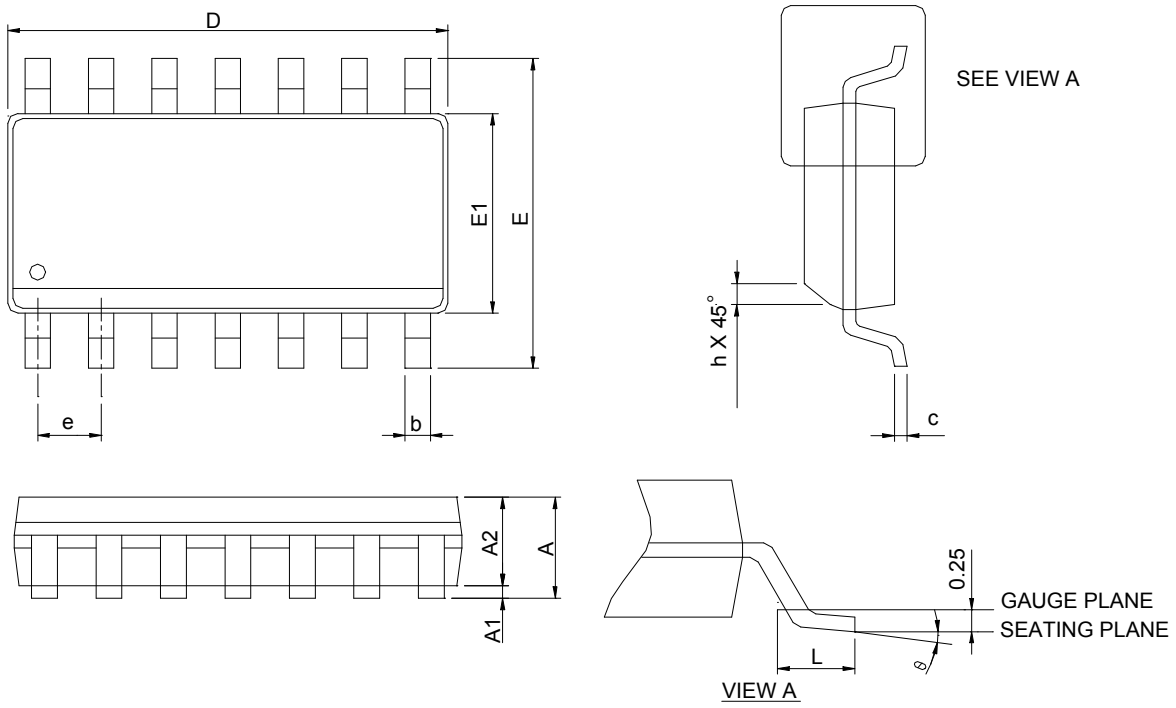


Figure 6. Layout Consideration

Package Information

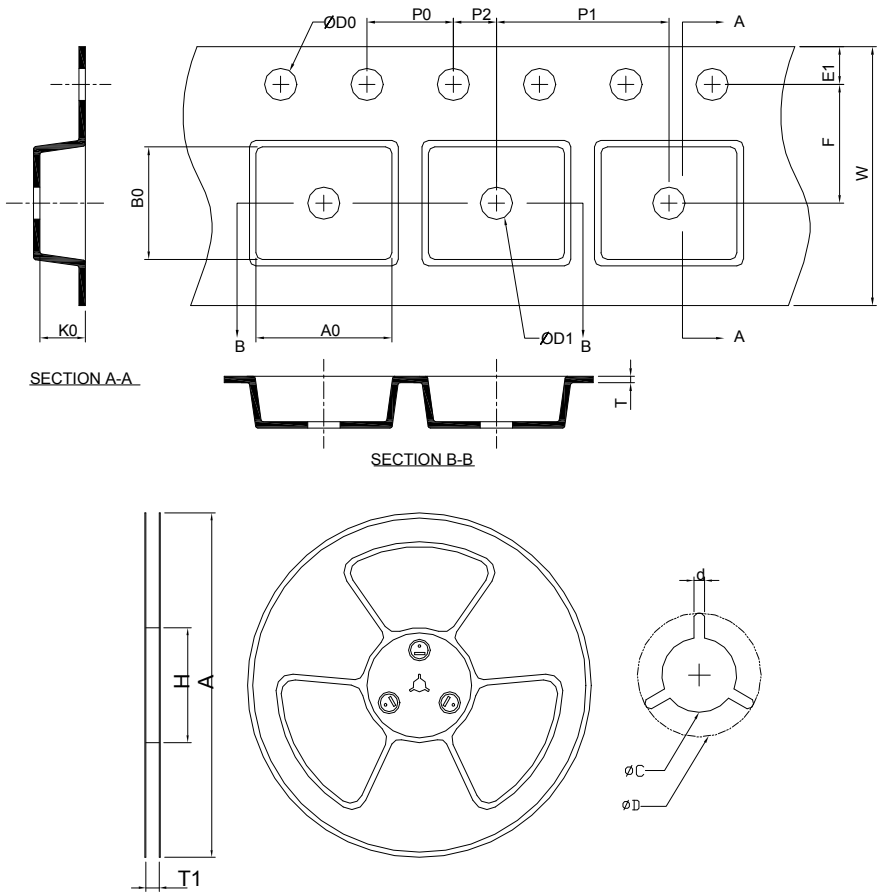
SOP-14



SYMBOL	SOP-14			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	8.55	8.75	0.337	0.344
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AB.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-14	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.50±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	9.00±0.20	2.10±0.20

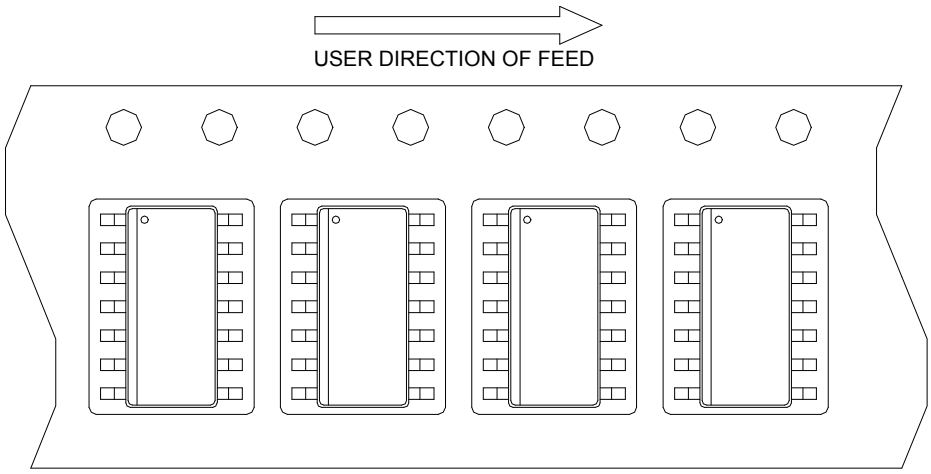
(mm)

Devices Per Unit

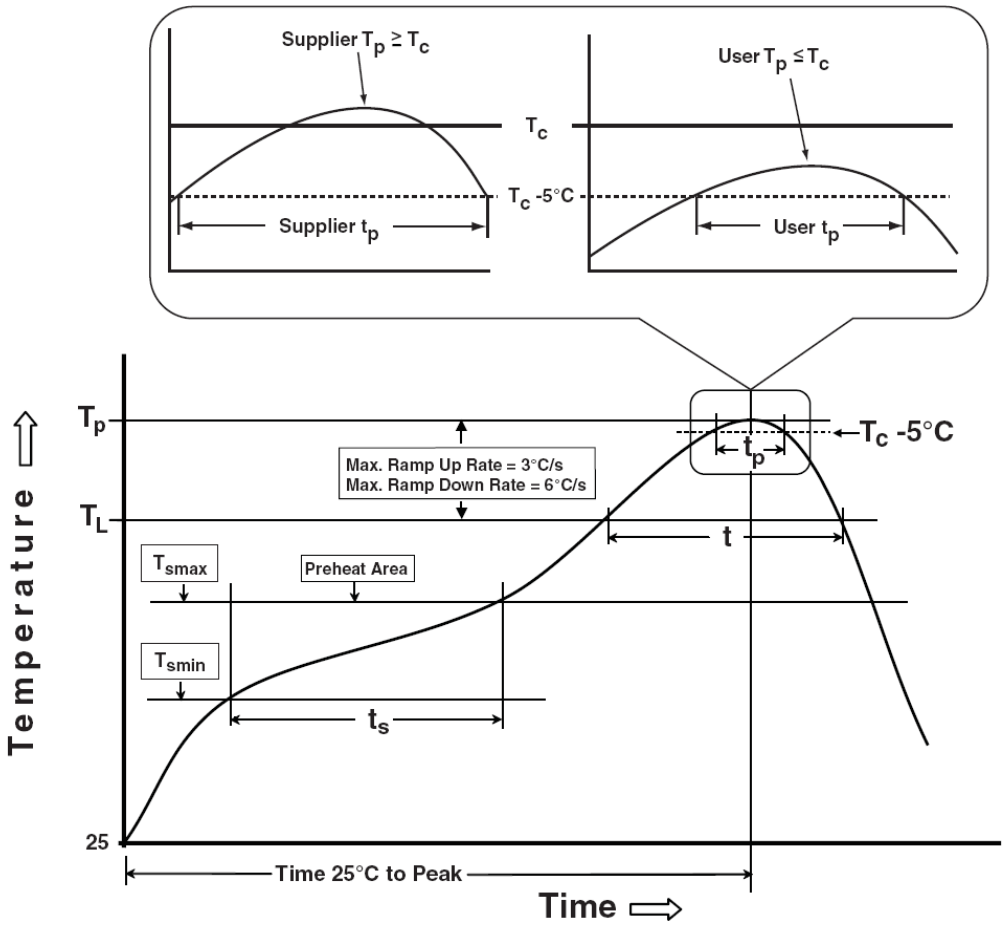
Package Type	Unit	Quantity
SOP-14	Tape & Reel	2500

Taping Direction Information

SOP-14



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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